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S12P MCU and Multifunctional Ignition and Injector Driver System In Package (SiP)

912_P812

SMALL ENGINE CONTROL SIP

98ASA00371D
100 Pin LQFP-EP

The MM912xP812 is an engine control IC combining an MCU (S12P) and analog control die (MC33812) intended for motorcycle and other single/dual cylinders small engine control applications.

The MCU S12P has 6 KB RAM, and flash memory size of 96 KB or 128 KB. The S12P family uses many of the same features found on the S12XS family, including error correction code (ECC) on flash memory, a separate data-flash module for diagnostic or data storage, a fast analog-to-digital converter (ATD), and a frequency modulated phase locked loop (IPLL) that improves the electromagnetic compatibility (EMC) performance.

The analog control IC consists of three integrated low side drivers, one pre-driver, a +5.0 V, voltage pre-regulator, an MCU watchdog circuit, an ISO 9141 K-Line interface, and a parallel interface for MCU communication. The three low side drivers are provided for driving a fuel injector, a lamp or LED, and a relay or another injector or fuel pump. The pre-driver is intended to drive either an insulated gate bipolar transistor (IGBT) or a bipolar Darlington transistor to control an ignition coil.

Features:

- Designed to operate over the range of ~4.7 V ≤ VPWR ≤ 36 V
- Relay/injector/fuel pump driver—current limit—4.0 A typical
- Lamp driver—current limit—1.5 A typical
- All external outputs protected against short to battery and over-current
- VCC voltage pre-regulator provides +5.0 V power for the MCU
- MCU watchdog timer circuit with parallel refresh/time setting line
- ISO-9141 K-Line transceiver for communicating diagnostic messages
- All signal lines are accessible
- Also available with MC9S12XEP100 MCU for calibration
- For detailed specifications see data sheets for the MC33812 and MC9S12Pxxx
- Provides single package ECU for minimum PC board area

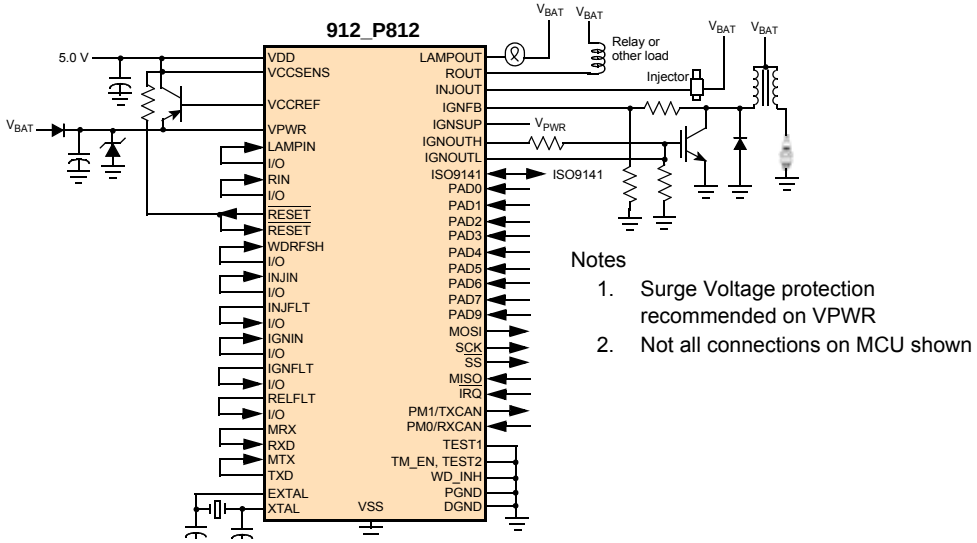

Figure 1. MM912_P812 Simplified Application Diagram

*This document contains certain information on a product under development.
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ORDERABLE PARTS

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.freescale.com and perform a part number search for the following device numbers.

Table 1. Orderable Part Variations

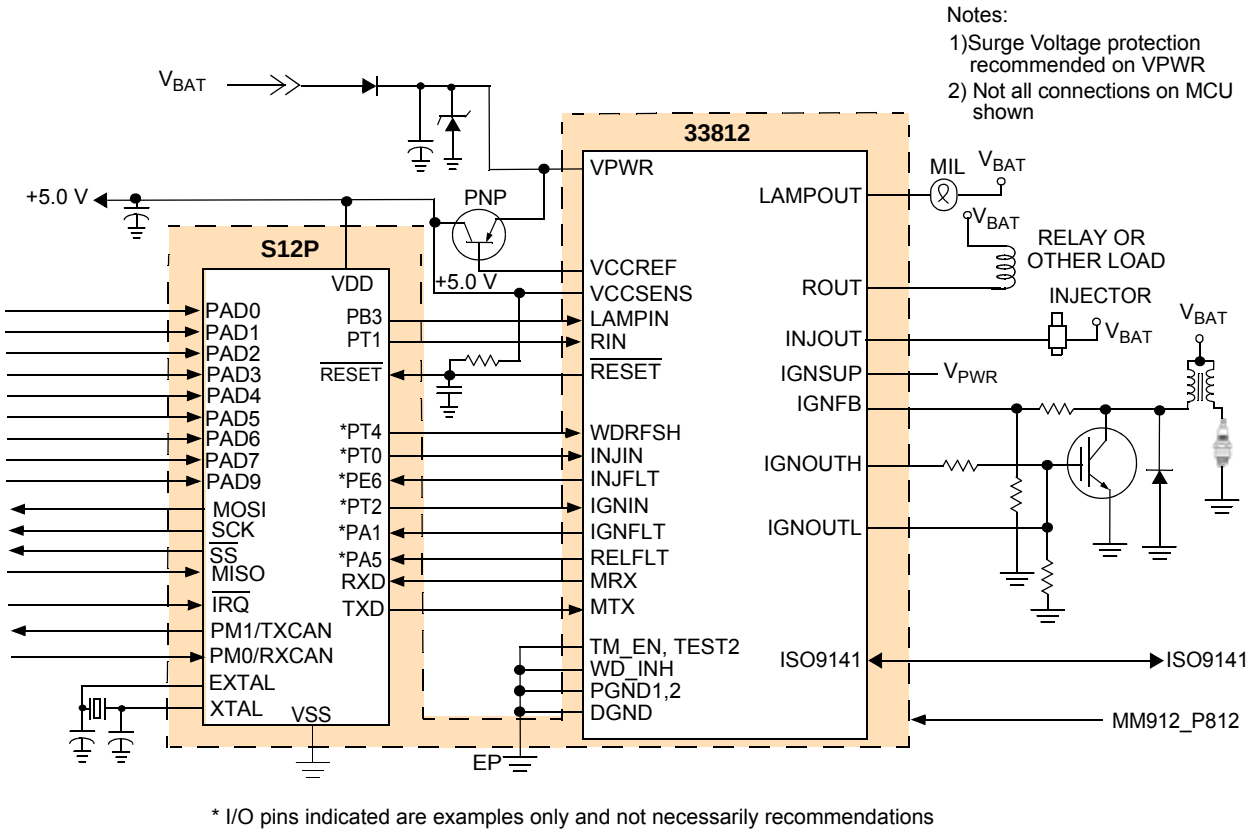
Part Number [3]	Processor Core	Flash Memory	RAM	Temperature (T_A)	Package
MM912IP812AMAF	S12P	96 k	6.0 k	-40 to 125 °C	100 pin LQFP
MM912JP812AMAF		128 k			

Notes

3. To Order parts in Tape & Reel, add the R2 suffix to the part number.

Table 2. Calibration Tools

Part Number	Processor Core	Contact
PM912NE812AMAF	S12XEP100	Contact Sales



* I/O pins indicated are examples only and not necessarily recommendations

Figure 2. MM912_P812 Detailed Application Diagram

PART IDENTIFICATION

This section provides an explanation of the part numbers and their alpha numeric breakdown.

DESCRIPTION

Part numbers for the chips have fields that identify the specific part configuration. You can use the values of these fields to determine the specific part you have received.

FORMAT AND EXAMPLES

Part numbers for a given device have the following format, followed by a device example:

Table 3 - Part Numbering - Analog EMBEDDED MCU + POWER:

MM 9 cc fpxxx rtv PPP RR - PM912JP812AMAF

FIELDS

These tables list the possible values for each field in the part number (not all combinations are valid).

Table 3. Part Numbering - Analog EMBEDDED MCU + POWER

FIELD	DESCRIPTION	VALUES
MM	Product Category	MM = Qualified Device PM = Prototype Device
9	Memory Type	9 = Flash, OTP
cc	Micro Core	12 = HC12
f	Memory Size	I = 96 k J = 128 k
p	Processor Core	P = S12P
xxx	Analog Core/Target	812 = MC33812
r	Revision	(default A)
t	Temperature Range	M = -40 °C to 125 °C
v	Variation	(default blank)
PPP	Package Designator	AF = 100 pin LQFP-EP
RR	Tape and Reel Indicator	R2 = Tape and Reel 13”

INTERNAL BLOCK DIAGRAM

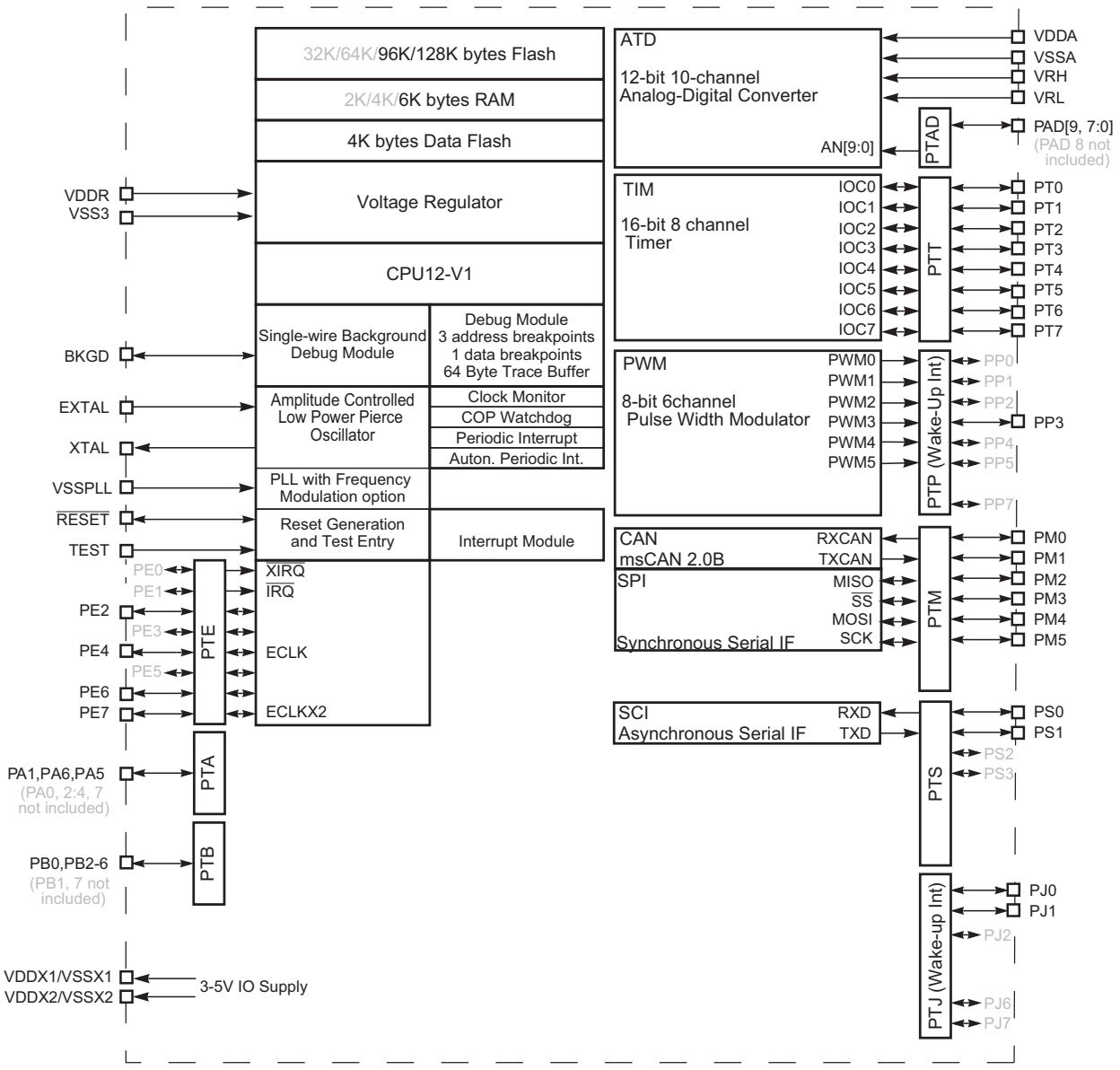
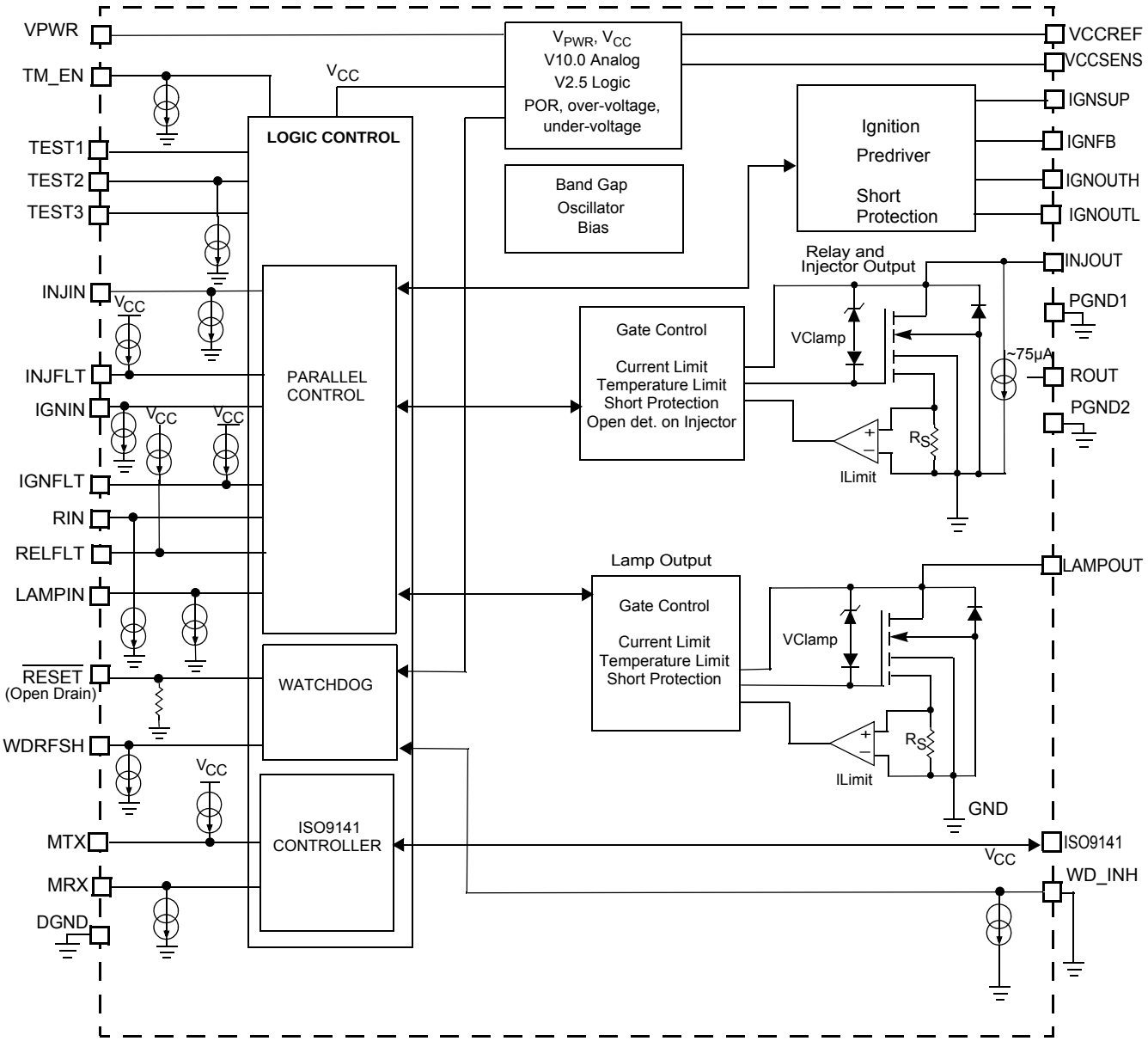


Figure 3. MC9S12P Family Block Diagram

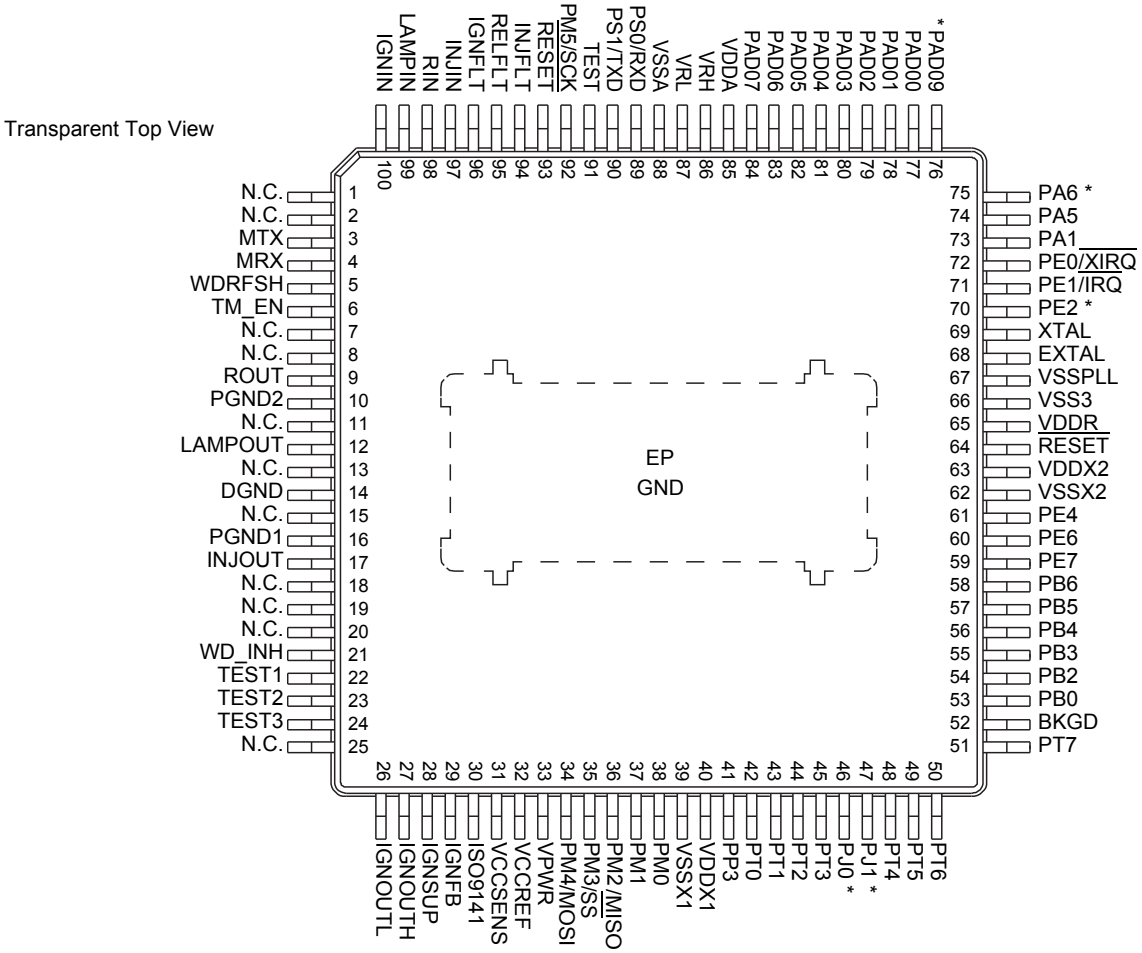


Notes

4. Pull-up and pull-down current sources are ~50 µA, unless otherwise noted

Figure 4. 33812 Simplified Internal Block Diagram

PIN CONNECTIONS



Notes

5. Pins denoted by an * are functionally different in calibration on the S12XEP100 device. If using both devices with the same PC board, be aware of the differences.
6. EP, PGND1, PGND2, and DGND, must all be connected to the ground plane.
7. Compared to the S12P in the 80 pin QFP package, 21 pins are missing in the SiP. These pins are: PP2, PP1, PP0, PB1, PB7, PE5, PJ2, PE3, PA0, PA2, PA3, PA4, PA7, PAD08, PS2, PS3, PJ7, PJ6, PP7, PP5, and PP4.

Figure 5. MM912_P812 Pin Connections

Table 4. MM912_P812 Pin Definitions

Analog or MCU	Pin	Pin Name	Pin Function	Formal Name	Description and Recommendations
-	1	N.C.	Unused	-------	Unused pin, leave open
-	2	N.C.	Unused	-------	Unused pin, leave open
Analog	3	MTX	Input	ISO9141 Data Input to MCU	Input logic level ISO9141 data, from the MCU, to the ISO9141 IN/OUT pin Connect to MCU SCI TXD output (pin 90) if using ISO9141 circuit
Analog	4	MRX	Output	ISO9141 Data Output to MCU	Output logic level ISO9141 data to the MCU from the ISO9141 IN/OUT pin Connect to MCU SCI RXD input (pin 89) if using ISO9141 circuit
Analog	5	WDRFSH	Input	Watchdog Refresh	Logic Level input from MCU to refresh the watchdog circuit to prevent $\overline{\text{RESET}}$ Connect to MCU I/O output (e.g. PT4 pin 48)
Analog	6	TM_EN	Input	Test Mode Enable	Used by Freescale test engineering, Connect to Ground
-	7	N.C.	Unused	-------	Unused pin, leave open
-	8	N.C.	Unused	-------	Unused pin, leave open
Analog	9	ROUT	Output	Relay Driver Output	Low side relay driver output driven by parallel input RIN Use ESD capacitor where the signal goes off the PC Board
Analog	10	PGND2	Ground	Power Ground 2	Ground for the RELAY driver output Connect to Ground
-	11	N.C.	Unused	-------	Unused pin, leave open
Analog	12	LAMPOUT	Output	Warning Lamp Output	Low side driver output for MIL (warning lamp) driven by parallel input LAMPIN. Use an ESD capacitor where the signal goes off the PC Board
-	13	N.C.	Unused	-------	Unused pin, leave open
Analog	14	DGND	Ground	Supply Ground	Used as ground for all low power signals. Connect to Ground
-	15	N.C.	Unused	-------	Unused pin, leave open
Analog	16	PGND1	Ground	Power Ground 1	Ground for INJOUT injector driver output. Connect to Ground
Analog	17	INJOUT	Output	Injector Driver Output	Low side driver output for the Injector driven by parallel input INJIN. Use an ESD capacitor where the signal goes off the PC Board.
-	18	N.C.	Unused	-------	Unused pin, leave open
-	19	N.C.	Unused	-------	Unused pin, leave open
-	20	N.C.	Unused	-------	Unused pin, leave open
Analog	21	WD_INH	Input	Watchdog Inhibit	Normally tied to GND, If tied high through a pull-up, it inhibits RESET from occurring when a watchdog timeout occurs. Normally connect to Ground.
Analog	22	TEST1	Input	Test 1	MUST be tied to GND. Connect to Ground
Analog	23	TEST2	Input	Test 2	MUST be tied to GND. Connect to Ground
Analog	24	TEST3	Input	Test 3	MUST leave OPEN. leave open
-	25	N.C.	Unused	-------	Unused pin, leave open
Analog	26	IGNOUTL	Output	Ignition Output Low	Low side output to drive the Gate/Base of the IGBT/Bipolar Darlington The network used on this pin is determined by the user requirements.
Analog	27	IGNOUTH	Output	Ignition Output High	High side output to drive the Gate/Base of IGBT/Bipolar Darlington The network used on this pin is determined by the user requirements.

Table 4. MM912_P812 Pin Definitions

Analog or MCU	Pin	Pin Name	Pin Function	Formal Name	Description and Recommendations
Analog	28	IGNSUP	Input	Ignition Output Supply	Tie to +5.0 V for Darlington, tie to the V_{PWR} supply for the IGBT output device
Analog	29	IGNFB	Input	Feedback from Source	Voltage feedback from the source of the Ignition driver transistor through a 10:1 voltage divider. Use a 10:1 voltage divider (36 k/4.02 k)
Analog	30	ISO9141	Input/ Output	ISO9141 K-Line Bidirectional Serial Data Signal	The ISO9141 pin is a V_{PWR} level IN/OUT signal connected to a external ECU Tester, using ISO9141 Protocol. The Output is Open drain and the Input is a ratiometric V_{PWR} level threshold comparator. Use an ESD capacitor where the signal goes off the PC Board.
Analog	31	VCCSENS	Input	Voltage Sense from VCC	Feedback to the internal VCC regulator from a external pass transistor. Must have the minimum of a 2.2 μF capacitor
Analog	32	VCCREF	Output	VCC Reference Base drive	Base drive voltage for an external PNP pass transistor
Analog	33	VPWR	Supply Input	Main Voltage Supply Input	VPWR is the main voltage supply input for the device. It connected to a +12 volt battery (It should have reverse battery protection and transient suppression.) It also needs a bypass capacitor to ground (100 nF or 0.1 μF)
MCU	34	PM4	I/O	PM4/ MOSI (SPI)	Port M, I/O pin 4 is a general purpose input or output pin. It can be configured as the master output (during master mode) or slave input pin (during slave mode). MOSI for the serial peripheral interface (SPI).
MCU	35	PM3	I/O	PM3/ $\overline{SS}$ (SPI)	Port M, I/O pin 3 is a general purpose input or output pin. It can be configured as the slave select output pin $\overline{SS}$ of the serial peripheral interface (SPI) (during master mode) and chip select input ($\overline{CS}$) (during slave mode).
MCU	36	PM2	I/O	PM2/ MISO (SPI)	Port M, I/O pin 2 is a general purpose input or output pin. It can be configured as the master input (during master mode) or slave output pin (during slave mode). MISO for the serial peripheral interface (SPI).
MCU	37	PM1	I/O	PM1/ TXCAN	Port M, I/O pin 1 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN of the scalable controller area network controller (CAN).
MCU	38	PM0	I/O	PM0/ RXCAN	Port M, I/O pin 0 is a general purpose input or output pin. It can be configured as the receive pin RXCAN of the scalable controller area network controller (CAN).
MCU	39	VSSX1	Ground	VSSX1	External ground for I/O drivers. Bypass requirements depend on how heavily the MCU pins are loaded. All VSSX pins are connected together internally. Connect to Ground
MCU	40	VDDX1	Supply Input	VDDX1	External power for I/O drivers. Bypass requirements depend on how heavily the MCU pins are loaded. All VDDX pins are connected together internally. Connect to VCC and use a 100 nF bypass capacitor to ground.
MCU	41	PP3	I/O	PP3/KWP3/PWM3	Port P, I/O pin 3 is a general purpose input or output pin. It can be configured as a keypad wake-up input. It can be configured as a pulse width modulator (PWM) output channel 3.
MCU	42	PT0	I/O	PT0/IOC0/PWM0	Port T, I/O pin 0 is a general purpose input or output pin. It can be configured as a timer (TIM) channel 0 or pulse width modulator (PWM) output channel 0.
MCU	43	PT1	I/O	PT1/IOC1	Port T, I/O pin 1 is a general purpose input or output pin. It can be configured as a timer (TIM) channel 1.
MCU	44	PT2	I/O	PT2/IOC2	Port T, I/O pin 2 is a general purpose input or output pin. It can be configured as a timer (TIM) channel 2.

Table 4. MM912_P812 Pin Definitions

Analog or MCU	Pin	Pin Name	Pin Function	Formal Name	Description and Recommendations
MCU	45	PT3	I/O	PT3/IOC3	Port T, I/O pin 3 is a general purpose input or output pin. It can be configured as a timer (TIM) channel 3.
MCU	46	PJ0 VDDF [8]	I/O Supply [8]	PJ0/KWJ0 VDDF 3.3 V supply output [8] (S12XEP100 ONLY)	Port J, I/O pin 0 is a general purpose input or output pin. It can be configured as a keypad wake-up input. (**Only on S12P, not on S12XEP100)** Signals VDDF/VSS are the secondary outputs of VREG_3V3 that provide the power supply for the NVM logic. These signals are connected to device pins to allow external decoupling capacitors (220 nF, X7R ceramic). In Shutdown mode an external supply driving VDDF/VSS can replace the voltage regulator. On S12XEP100. [8]
MCU	47	PJ1 VSS1 [8]	I/O Ground [8]	PJ1/KWJ1 VSS1 [8]	Port J, I/O pin 1 is a general purpose input or output pin. It can be configured as a keypad wake-up input (**Only on S12P, not on S12XEP100)** See previous description for VDDF/VSS. Only on S12XEP100 [8]
MCU	48	PT4	I/O	PT4/IOC4/PWM4	Port T, I/O pin 4 is a general purpose input or output pin. It can be configured as a timer (TIM) channel 4 or pulse width modulator (PWM) output 4.
MCU	49	PT5	I/O	PT5/IOC5/PWM5/ API_EXTCLK	Port T, I/O pin 5 is a general purpose input or output pin. It can be configured as a timer (TIM) channel 5, pulse width modulator (PWM) output 5, or as the output of the API_EXTCLK.
MCU	50	PT6	I/O	PT6/IOC6	Port T, I/O pin 6 is a general purpose input or output pin. It can be configured as a timer (TIM) channel 6.
MCU	51	PT7	I/O	PT7/IOC7	Port T, I/O pin 7 is a general purpose input or output pin. It can be configured as a timer (TIM) channel 7.
MCU	52	BKGD	BDM	BKGD/MODC	The BKGD/MODC pin is used as a pseudo open-drain pin for the background debug communication. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. The BKGD pin has an internal pull-up device.
MCU	53	PB0	I/O	PB0	Port B, I/O pin 0 is a general purpose input or output pin.
MCU	54	PB2	I/O	PB2	Port B, I/O pin 2 is a general purpose input or output pin.
MCU	55	PB3	I/O	PB3	Port B, I/O pin 3 is a general purpose input or output pin.
MCU	56	PB4	I/O	PB4	Port B, I/O pin 4 is a general purpose input or output pin.
MCU	57	PB5	I/O	PB5	Port B, I/O pin 5 is a general purpose input or output pin.
MCU	58	PB6	I/O	PB6	Port B, I/O pin 6 is a general purpose input or output pin.
MCU	59	PE7	I/O	PE7/ECLKX2	Port E, I/O pin 7 is a general purpose input or output pin. An internal pull-up is enabled during reset. It can be configured to output ECLKX2.
MCU	60	PE6	I/O	PE6	Port E, I/O pin 6 is a general purpose input or output pin.
MCU	61	PE4	I/O	PE4/ECLK	Port E, I/O pin 4 is a general purpose input or output pin. It can be configured to drive the internal bus clock ECLK. ECLK can be used as a timing reference. The ECLK output has a programmable prescaler.
MCU	62	VSSX2	Ground	VSSX2	External ground for I/O drivers. Bypass requirements depend on how heavily the MCU pins are loaded. All VSSX pins are connected together internally. Connect to Ground
MCU	63	VDDX2	Supply Input	VDDX2	External power for I/O drivers. Bypass requirements depend on how heavily the MCU pins are loaded. All VDDX pins are connected together internally. Connect to VCC and use a 100 nF bypass capacitor to Ground

Table 4. MM912_P812 Pin Definitions

Analog or MCU	Pin	Pin Name	Pin Function	Formal Name	Description and Recommendations
Notes	Notes				
	8. S12XEP100 signal noted for reuse of PC board for the calibration device.				
MCU	64	$\overline{\text{RESET}}$	Input	$\overline{\text{RESET}}$ External Reset Pin	The $\overline{\text{RESET}}$ pin is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. The $\overline{\text{RESET}}$ pin has an internal pull-up device. Use external pull-up (10 k and 100 pF capacitor to Ground) connect to the 33812 $\overline{\text{RESET}}$ pin 93.
MCU	65	VDDR	Supply Input	VDDR	Power supply input to the internal voltage regulator. Connect to VCC and use bypass capacitor, 100 nF to Ground.
MCU	66	VSS3	Ground	VSS3 Core Ground Pin	The voltage supply of nominally 1.8 V is derived from the internal voltage regulator. The return current path is through the VSS3 pin. No static external loading of these pins is permitted. Connect to Ground
MCU	67	VSSPLL	Ground	VSSPLL PLL Ground Pin	Provides operating voltage and ground for the phased-locked loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground are generated by the internal regulator. Connect to Ground
MCU	68	EXTAL	Clock Input	EXTAL Oscillator Pin	EXTAL is the external clock pin. On reset all the device clocks are derived from the internal reference clock. Connect to external crystal and 18 pf capacitor to Ground
MCU	69	XTAL	Clock Output	XTAL Oscillator Pin	XTAL is the crystal driver pin. On reset all the device clocks are derived from the internal reference clock. XTAL is the oscillator output. Connect to external crystal and 18 pf capacitor to Ground
MCU	70	PE2 VDDPLL [9]	I/O PLL Supply [9]	PE2 Output of 3.3 V regulator [9]	Port E, I/O pin 2 is a general purpose input or output pin. (**Only on S12P, not on S12XEP100)** Signals VDDPLL/VSSPLL are the secondary outputs of VREG_3V3 that provide the power supply for the PLL and oscillator. These signals are connected to device pins to allow external decoupling capacitors. (100 nF...220 nF, X7R ceramic). In Shutdown mode, an external supply driving VDDPLL/VSSPLL can replace the voltage regulator. **Only on S12XEP100** [9]
MCU	71	$\overline{\text{IRQ}}$	I/O	PE1/$\overline{\text{IRQ}}$	Port E, I/O pin 1 is a general purpose input pin and the maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake-up the MCU from stop or wait mode.
MCU	72	$\overline{\text{XIRQ}}$	I/O	PE0/$\overline{\text{XIRQ}}$	Port E, I/O pin 0 is a general purpose input pin and the non-maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake-up the MCU from stop or wait mode. The XIRQ interrupt is level sensitive and active low. As XIRQ is level sensitive while this pin is low, the MCU will not enter STOP mode. Connect to 10K pull-up resistor to VCC.
MCU	73	PA1	I/O	PA1	Port A, I/O pin 1 is a general purpose input or output pin.
MCU	74	PA5	I/O	PA5	Port A, I/O pin 5 is a general purpose input or output pin.
MCU	75	PA6 VDD [9]	I/O Supply [9]	PA6 ON S12P Output of 3.3 V regulator [9]	Port A, I/O pin 6 is a general purpose input or output pin. (**Only on S12P, not on S12XEP100)** Signals VDD/VSS2 are the primary outputs of VREG_3V3 that provide the power supply for the core logic. These signals are connected to device pins to allow external decoupling capacitors (220 nF, X7R ceramic). In Shutdown mode, an external supply driving VDD/VSS2 can replace the voltage regulator. **Only on S12XEP100** [9]

Notes

9. S12XEP100 signal noted for reuse of PC board for the calibration device.

Table 4. MM912_P812 Pin Definitions

Analog or MCU	Pin	Pin Name	Pin Function	Formal Name	Description and Recommendations
MCU	76	PAD09 VSS2 (10)	A/D Input Ground (10)	PAD09 ON S12P Ground of 3.3 V regulator (10)	PAD09 is the general purpose input or output pin and analog input of the analog-to-digital converter, A/D Use voltage divider if necessary, and ESD protection capacitor. Use of low pass filter as necessary. **(Only on S12P, not on S12XEP100)** **See description of VDD above. Only on S12XEP100 (9)**
MCU	77	PAD00	A/D Input	PAD00	PAD00 is the general purpose input or output pin and analog input AN0 of the analog-to-digital converter, A/D. Use voltage divider if necessary, and ESD protection capacitor. Use of low pass filter as necessary.
MCU	78	PAD01	A/D Input	PAD01	PAD01 is the general purpose input or output pin and analog input AN1 of the analog-to-digital converter, A/D. Use voltage divider if necessary, and ESD protection capacitor. Use of low pass filter as necessary.
MCU	79	PAD02	A/D Input	PAD02	PAD02 is the general purpose input or output pin and analog input AN2 of the analog-to-digital converter, A/D. Use voltage divider if necessary, and ESD protection capacitor. Use of low pass filter as necessary.
MCU	80	PAD03	A/D Input	PAD03	PAD03 is the general purpose input or output pin and analog input AN3 of the analog-to-digital converter, A/D. Use voltage divider if necessary, and ESD protection capacitor. Use of low pass filter as necessary.
MCU	81	PAD04	A/D Input	PAD04	PAD04 is the general purpose input or output pin and analog input AN4 of the analog-to-digital converter, A/D. Use voltage divider if necessary, and ESD protection capacitor. Use of low pass filter as necessary.
MCU	82	PAD05	A/D Input	PAD05	PAD05 is the general purpose input or output pin and analog input AN5 of the analog-to-digital converter, A/D. Use voltage divider if necessary, and ESD protection capacitor. Use of low pass filter as necessary.
MCU	83	PAD06	A/D Input	PAD06	PAD06 is the general purpose input or output pin and analog input AN6 of the analog-to-digital converter, A/D. Use voltage divider if necessary, and ESD protection capacitor. Use of low pass filter as necessary.
MCU	84	PAD07	A/D Input	PAD07	PAD07 is the general purpose input or output pin and analog input AN7 of the analog-to-digital converter, A/D. Use voltage divider if necessary, and ESD protection capacitor. Use of low pass filter as necessary.
MCU	85	VDDA	Supply Input	VDDA	This is the power supply input pin for the analog-to-digital converter and the voltage regulator. Connect to VCC and use a bypass capacitor, 100 nF to Ground.
MCU	86	VRH	Supply Input	VRH	VRH and VRL are the reference voltage input pins for the analog-to-digital converter. Connect to VCC and use a bypass capacitor, 100 nF to Ground.
MCU	87	VRL	Supply Input	VRL	VRH and VRL are the reference voltage input pins for the analog-to-digital converter. Connect to Ground.
MCU	88	VSSA	Ground	VSSA	This is the ground input pin for the analog-to-digital converter and the voltage regulator. Connect to Ground.
MCU	89	PS0/RXD	I/O	PS0/ RXD (SCI)	Port S, I/O pin 0 is a general purpose input or output pin. It can be configured as the receive pin RXD of serial communication interface (SCI). If used for ISO9141 connect to pin 4, MRX.

Notes

10. S12XEP100 signal noted for reuse of PC board for the calibration device.

Table 4. MM912_P812 Pin Definitions

Analog or MCU	Pin	Pin Name	Pin Function	Formal Name	Description and Recommendations
MCU	90	PS1/TXD	I/O	PS1/ TXD (SCI)	Port S, I/O pin 1 is a general purpose input or output pin. It can be configured as the receive pin TXD of serial communication interface (SCI). If used for ISO9141 connect to pin 3, MTX.
MCU	91	TEST	Input	Test	MUST leave OPEN. leave open
MCU	92	PM5/SCK	I/O	PM5/ SCK (SPI)	Port M, I/O pin 5 is a general purpose input or output pin. It can be configured as the serial clock input pin for the serial peripheral interface (SPI) when the SPI is in slave mode and as a serial clock output when the SPI is in master mode.
Analog	93	$\overline{\text{RESET}}$	Output	$\overline{\text{RESET}}$ Output to MCU	Logic Level $\overline{\text{Reset}}$ signal used to reset the MCU when the watchdog circuit times out, during under-voltage condition on VCC, and for initial power up and power down. Provides $\overline{\text{RESET}}$ to MCU on pin 64.
Analog	94	INJFLT	Output	Injector Fault	Logic Level output to MCU indicating any fault in the injector circuit.
Analog	95	RELFLT	Output	Relay Fault	Logic Level output to MCU indicating any fault in the relay circuit.
Analog	96	IGNFLT	Output	Ignition Fault	Logic Level output to MCU indicating any fault in the ignition circuit.
Analog	97	INJIN	Input	Injector Parallel Input	Logic Level Parallel input from the MCU to control the injector driver output
Analog	98	RIN	Input	Relay Parallel Input	Logic Level Parallel input to activate RELAY output, ROUT
Analog	99	LAMPIN	Input	LAMP Parallel Input	Logic Level Parallel input to activate the malfunction indicator lamp output, LAMP
Analog	100	IGNIN	Input	Ignition Parallel Input	Logic Level Parallel input from MCU controlling the ignition coil current flow and spark.
-	EP	GND	Ground	Substrate Ground	Should be tied to the Ground plane. Connect to Ground.

Calibration:

Note that Pins 46,47,70,75, and 76 are different between the S12P and the S12XEP100 SiPs.

For the S12P, these pins can be used as I/O:

Pin 46 = PJ0, Pin 47 = PJ1, Pin 70 = PE2, Pin 75 = PA6, Pin 76 = PAD09

For the S12XEP100, there must be:

100 nF, X7R ceramic capacitor between Pin 46 and 47

220 nF, X7R ceramic capacitor between Pin 67 and 70

220 nF, X7R ceramic capacitor between Pin 75 and 76

In order to have the same PC Board for both SiPs, it is necessary to place the pads for the three capacitors on the PC Board, and use 0 ohm resistors to connect the 5 I/O (for the S12P) to the external circuitry. When the S12XEP100 is used, the capacitors will be populated and the 0 ohm resistors will not be populated. When populated, if the I/O signals are not needed, then the 0 ohm resistors can be eliminated and only the capacitors are needed for the S12XEP100 boards.

MAXIMUM RATINGS

Table 5. MM912_P812 Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Rating	Value	Unit	Notes
ELECTRICAL RATINGS				
	ESD Voltage		V	(11)
V_{ESD1}	Human Body Model	±2000		
V_{ESD2}	Machine Model	±200		
V_{ESD3}	Charge Device Model (Corner pins)	±750		
V_{ESD4}	Charge Device Model	±500		
THERMAL RATINGS				
	Operating Temperature		°C	
T_A	Ambient	-40 to 125		
T_J	Junction	-40 to 150		
T_C	Case	-40 to 125		
T_{STG}	Storage Temperature	-55 to 150	°C	
P_D	Power Dissipation (T_A = 25°C)	1.7	W	(14)
T_{SOLDER}	Peak Package Reflow Temperature During Solder Mounting	Note 13	°C	(12), (13)
	Thermal Resistance		°C/W	
$R_{\theta JA}$	Junction-to-Ambient	75		
$R_{\theta JL}$	Junction- to-Lead	8.0		
$R_{\theta JC}$	Junction-to-Flag	1.2		

Notes

11. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
12. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
13. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.
14. This parameter is guaranteed by design but is not production tested.

ANALOG MC33812 PARAMETRICS

The detailed MC33812 specifications can be found in the MC33812 data sheet. See MC33812.

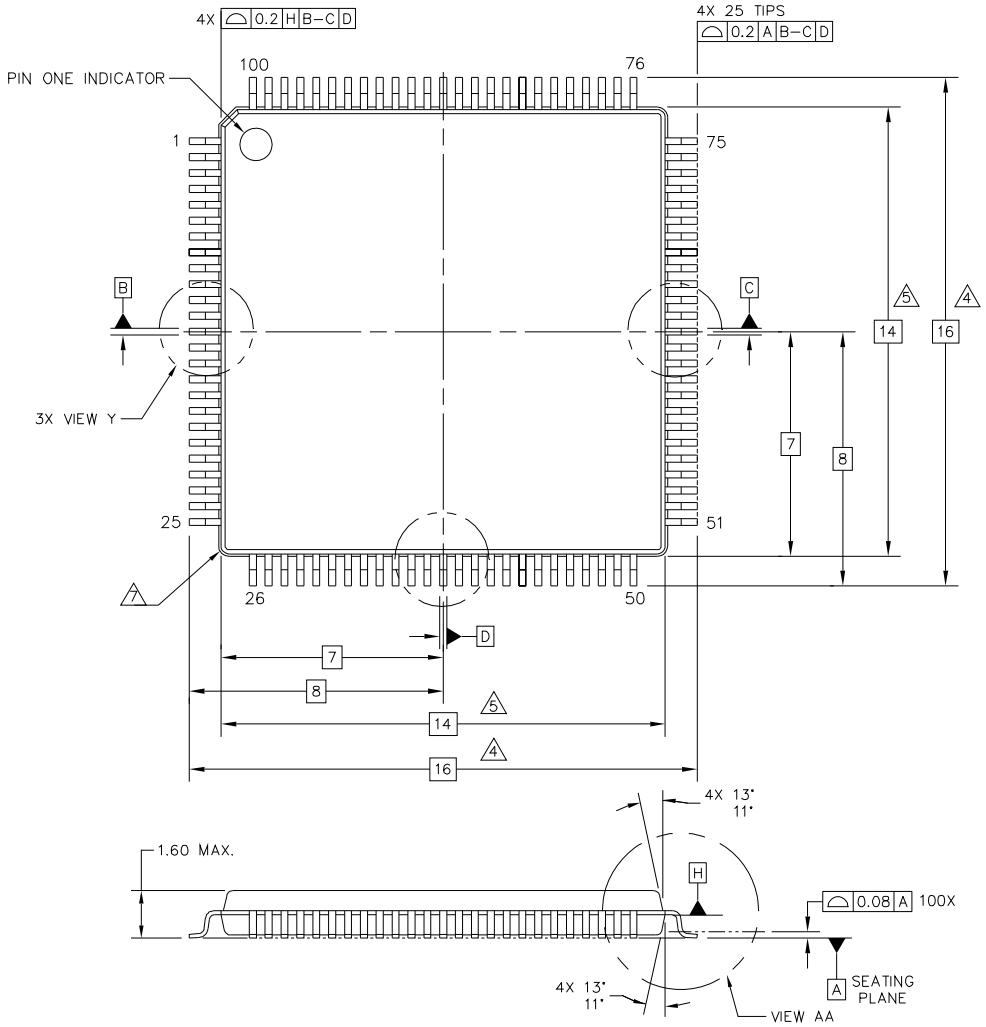
MICROCONTROLLER S12P PARAMETRICS

The detailed S12P specifications can be found in the MC9S12P128 reference manual. See MC9S12P128.

PACKAGING

PACKAGING DIMENSIONS

Important: For the most current revision of the package, visit www.freescale.com and perform a keyword search on 98ASA00371D.



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	CASE NUMBER: 2218–01	15 JUN 2011
	STANDARD: NON–JEDEC	

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100-PIN
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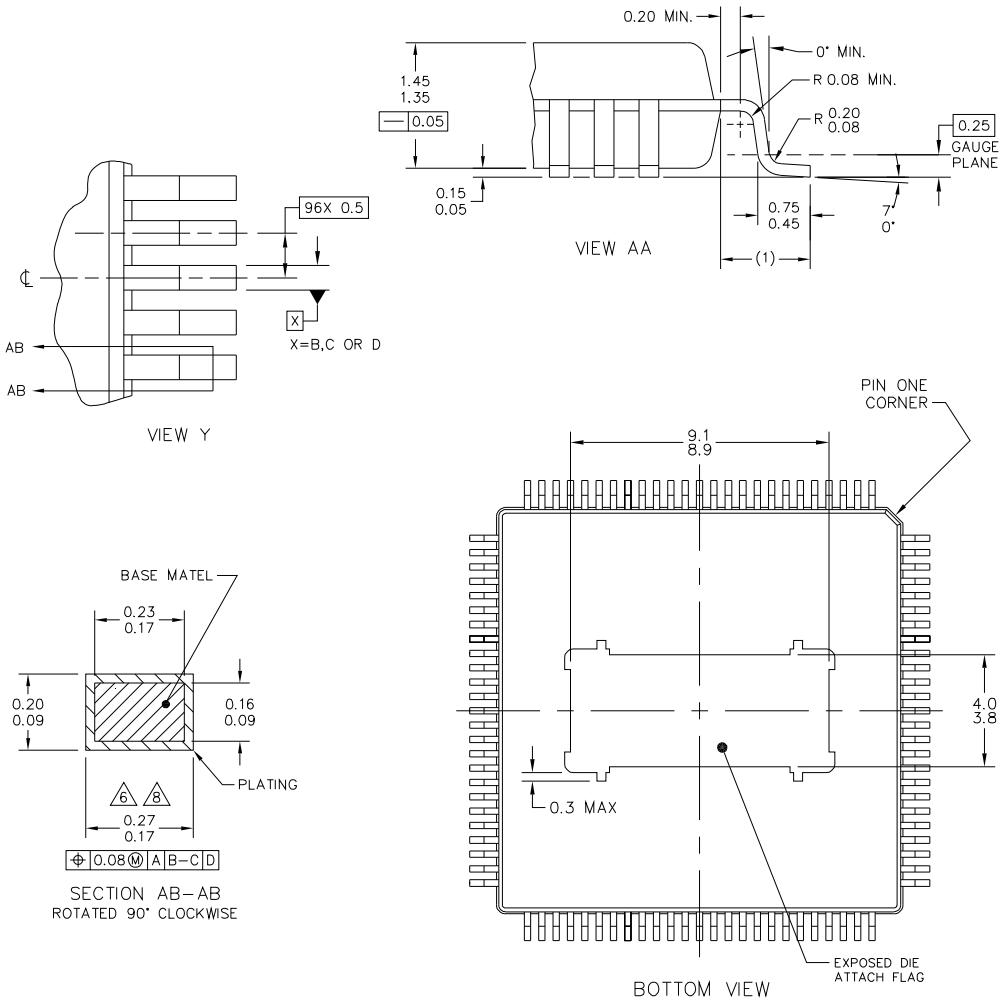
ISSUE 0



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NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS B–C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THESE DIMENSIONS TO BE DETERMINED AT SEATING PLANE, DATUM A.
5. THESE DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 PER SIDE. THESE DIMENSIONS DO INCLUDE MOLD MISMATCH. THESE DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE H..
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10MM AND 0.25MM FROM THE LEAD TIP.

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REFERENCES

DOCUMENT	URL
MC33812 Datasheet	• http://www.freescale.com/files/analog/doc/data_sheet/MC33812.pdf
MC9S12P128 Reference Manual	• http://www.freescale.com/files/microcontrollers/doc/data_sheet/MC9S12P128.pdf
SG187 Selector Guide	• http://www.freescale.com/files/microcontrollers/doc/selector_guide/SG187.pdf
SG1002 Selector Guide	• http://www.freescale.com/files/shared/doc/selector_guide/SG1002.pdf
Application Note AN4388	• http://www.freescale.com/files/analog/doc/app_note/AN4388.pdf

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	5/2012	• Initial release

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